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(54) Method and apparatus for updating coefficients in a complex adaptive equalizer

Verfahren und Einrichtung zur Aktualisierung der Koeffizienten eines komplexen, adaptiven Entzerrers

Procédé et dispositif pour la mise à jour des coéfficients d'un égalisateur complexe adaptatif

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Description

The present invention relates to digital communications, and more particularly to an improved adaptive equalizer for reducing intersymbol interference in a received signal.

The invention in particular relates to a method for updating coefficients for input to a filter stage of an adaptive equalizer, said filter stage receiving one of said updated coefficients during each one of successive filter clock cycles, said coefficients being updated in response to error signals derived from equalized data output from said adaptive equalizer.

The invention further relates to an adaptive equalizer apparatus comprising a filter stage, said filter stage receiving one of the updated coefficients during each one of successive filter clock cycles, and updating means for updating said coefficients in response to error signals derived from equalizer data output from said adaptive equalizer.

Digital data, for example digitized video for use in broadcasting high definition television (HDTV) signals, can be transmitted over terrestrial very high frequency (VHF) or ultra high frequency (UHF) analog channels for communication to end users. Analog channels deliver corrupted and transformed versions of their input waveforms. Corruption of the waveform, usually statistical, may be additive and/or multiplicative, because of possible background thermal noise, impulse noise, and fades. Transformations performed by the channel are frequency translation, nonlinear or harmonic distortion, and time dispersion.

In order to communicate digital data via an analog channel, the data is modulated using, for example, a form of pulse amplitude modulation (PAM). Typically, quadrature amplitude modulation (QAM) is used to increase the amount of data that can be transmitted within an available channel bandwidth. QAM is a form of PAM in which a plurality, such as sixteen or thirty-two, bits of information are transmitted together in a pattern referred to as a "constellation".

In pulse amplitude modulation, each signal is a pulse whose amplitude level is determined by a transmitted symbol. In 16-QAM, symbol amplitudes of -3, -1, 1 and 3 in each quadrature channel are typically used. In bandwidth efficient digital communication systems, the effect of each symbol transmitted over a time-dispersive channel extends beyond the time interval used to represent that symbol. The distortion caused by the resulting overlap of received symbols is called intersymbol interference (ISI). This distortion has been one of the major obstacles to reliable high speed data transmission over low background noise channels of limited bandwidth. A device known as an "equalizer" is used to deal with the ISI problem.

In order to reduce the intersymbol interference introduced by a communication channel, rather precise equalization is required. Furthermore, the channel characteristics are typically not known beforehand. Thus, it is common to design and use a compromise (or a statistical) equalizer that compensates for the average of the range of expected channel amplitude and delay characteristics. A least mean square (LMS) error adaptive filtering scheme has been in common use as an adaptive equalization algorithm for over 20 years. This algorithm is described in B. Widrow and M. E. Hoff, Jr., "Adaptive Switching Circuits" in IRE Wescon Conv. Rec., Part 4, pp. 96-104, Aug. 1960. The use of the LMS algorithm in an adaptive equalizer to reduce intersymbol interference is discussed in S. U. H. Qureshi, "Adaptive Equalization", Proc. IEEE, Vol. 73, No. 9, pp. 1349-1387, September 1987.

In an LMS equalizer, the equalizer filter coefficients are chosen to minimize the mean square error, i.e., the sum of squares of all the ISI terms plus the noise power at the output of the equalizer. Therefore, the LMS equalizer maximizes the signal-to-distortion ratio at its output within the constraints of the equalizer time span and the delay through the equalizer. Before regular data transmission begins, automatic synthesis of the LMS equalizer for unknown channels may be carried out during a training period. This generally involves the iterative solution of a set of simultaneous equations. During the training period, a known signal is transmitted and a synchronized version of the signal is generated in the receiver to acquire information about the channel characteristics. The training signal may consist of periodic isolated pulses or a continuous sequence with a broad, uniform spectrum such as a widely known maximum length shift register or pseudo-noise sequence.

An important aspect of equalizer performance is its convergence, which is generally measured by the amount of time in symbol periods required for the error variance in the equalizer to settle at a minimum level, which is ideally zero. In order to obtain the most efficient operation for a data receiver, the equalizer convergence time must be minimized.

After any initial training period, the coefficients of an adaptive equalizer may be continually adjusted in a decision directed manner. In this mode, the error signal is derived from the final receiver estimate (not necessarily correct) of the transmitted sequence. In normal operation, the receiver decisions are correct with high probability, so that the error estimates are correct often enough to allow the adaptive equalizer to maintain precise equalization. Moreover, a decision directed adaptive equalizer can track slow variations in the channel characteristics or linear perturbations in the receiver front end, such as slow jitter in the sampler phase.

The larger the step size, the faster the equalizer tracking capability. However, a compromise must be made between fast tracking and the excess mean square error (MSE) of the equalizer. The excess MSE is that part of the error power in excess of the minimum attainable MSE (with tap gains frozen at their optimum settings). This excess MSE, caused by tap gains wan-

dering around the optimum settings, is directly proportional to the number of equalizer coefficients, the step size, and the channel noise power.

Many transmission systems employ modulation schemes that are constructed with complex signal sets. In other words, the signals are viewed as vectors in the complex plane, with the real axis called the inphase (I) channel and the imaginary axis called the quadrature (Q) channel. Consequently, when these signals are subjected to channel distortion and receiver impairments, cross talk between the I and Q channels occurs, requiring a complex adaptive equalizer. In this case, the equalizer's coefficients will be complex valued. If, as noted above, the channel distortion is unknown by the receiver, then the coefficients must be adjusted after the system has been in operation to cancel the channel distortion. The term "adaptive" in a complex adaptive equalizer signifies the ongoing adjustment of the coefficients.

Prior art adaptive equalizers, including complex adaptive equalizers, have suffered from a relatively long convergence time of the LMS algorithm. Alternate algorithms, such as the recursive least squares (RLS) algorithm have been developed in order to overcome this disadvantage, and the RLS algorithm does indeed converge faster than LMS. However, RLS is more complex to implement than LMS and there are also numerical stability problems associated with the RLS algorithm. Therefore, prior art designs have tolerated the longer convergence time of the LMS implementation in order to avoid the disadvantages of the RLS scheme.

Even though the LMS algorithm is less complex to implement than other algorithms such as RLS, substantial hardware is still required to implement the algorithm in systems where floating point signal processors are not fast enough.

International Journal of Electronics, Vol. 55, No. 3, September 1983, pages 473 - 477, Rao B.V. et al.: "A New Design for Digital Adaptive Filters" discloses an adaptive equalizer according to which every filter clock cycle only one equalizer coefficient is updated.

US 4,435,823 only relates to a FIR filter and discloses parallel processing in connection with the outputs from the FIR filter delays.

IEEE Journal on Selected Areas in Communications, Vol. SAC-5, No. 3, April 1987, New York, NY, US, pages 466 - 475, Baccetti B. et al.: "Full Digital Adaptive Equalization in 64-QAM Radio Systems" discloses the digital implementation of a baseband adaptive equalizer.

The object of the present invention is to provide a method and an adaptive equalizer in which the LMS algorithm is implemented such that hardware is minimized without sacrificing system performance.

This object is solved by a method for updating coefficients for input to a filter stage of an adaptive equalizer, said filter stage receiving one of said updated coefficients during each one of successive filter clock cycles, said coefficients being updated in response to error signals derived from equalized data output from said adaptive equalizer,

wherein according to the invention a pluarality of said coefficients are updated concurrently during each filter clock cycle by passing unequalized data through N successive delay elements to provide a delayed sample of the unequalized data from each of the delay elements;
the product of each delayed sample output from the delay elements and an error signal derived from equalized data output from said adaptive equalizer is obtained;
the product corresponding to each delay element is combined with previous product data corresponding to that delay element to produce N updated coefficients during each of said filter clock cycles; and during each successive filter clock cycle, one of the N coefficients updated during that cycle is input to said filter stage.

Further advantages embodiments of said method are subject matter of subclaims 2 to 6.

The object is further solved by an adaptive equalizer apparatus comprising a filter stage, said filter stage receiving one of the updated coefficients during each one of successive filter clock cycles,

updating means for updating said coefficients in response to error signals derived from equalizer data output from said adaptive equalizer
wherein according to the invention
said updating means comprise a plurality of successive delay elements coupled together to provide a plurality of delayed samples of unequalized signal data which are output for use in updating said coefficients;
means are provided for multiplying the delayed samples output from said delay elements by an error signal derived from equalized data output from said adaptive equalizer, said multiplying means providing a product corresponding to each delay element;
means are provided for combining the product corresponding to each delay element with previous product data corresponding to that delay element to concurrently produce an updated coefficient corresponding to each delay element during each of said filter clock cycles; and
means are provided for inputting to said filter stage during each successive filter clock cycle, the updated coefficient corresponding to one of said delay elements.

Further advantageous embodiments are subject matter of subclaims 8 to 17.

The present invention provides an advantageous implementation of the LMS algorithm that minimizes

hardware without sacrificing system performance.

In addition the present invention provides an advantageous LMS adaptive equalizer having improved convergence performance (i.e., faster convergence time) without undue added complexity.

Further the invention provides an advantageous adaptive equalizer that is easily implemented in an integrated circuit, such as in a very large scale integration (VLSI) device.

In accordance with the present invention, a method is provided for updating coefficients in a complex adaptive equalizer.

In a preferred embodiment complex signal data is passed through a plurality of successive delay stages to provide N sets of delayed complex signal data. The product of each set and a complex error signal is obtained, and each product is concurrently updated with previous product data for the set to provide N sets of updated complex coefficients for selective input to equalizer filters. By concurrently updating the products derived from each successive delay stage and the error signal, the covergence time of the equalizer is substantially reduced.

In a further preferred embodiment, the complex coefficients of each updated set are truncated, and the gain thereof is adjusted to provide coefficients at a suitable level for filtering by the equalizer filters. The sets of adjusted, truncated coefficients are multiplexed to provide a clocked stream of coefficient sets for input to the equalizer filters.

The present invention also provides apparatus for updating coefficients in an adaptive equalizer.

In a preferred embodiment a plurality of successive delay stages are coupled to provide a plurality of sets of delayed signal data from an input signal. Means are provided for multiplying each set of delayed signal data by an error signal to provide a plurality of products. Means concurrently update each product with previous product data to provide a plurality of sets of updated coefficients. The updated coefficient sets are selectively input to an equalizer filter stage.

In an illustrated embodiment, the update means comprise a plurality of parallel processing paths, each for updating one of said products. Each parallel processing path is coupled between the multiplying means and means for selectively inputting the updated coefficient sets to the equalizer filter stage. Each of the parallel processing paths comprises an adder having a first input for receiving a product from the multiplying means, a second input and an output. A delay circuit is coupled to receive product data from the adder output and to couple delayed product data to the second adder input. Means are provided for coupling the adder output to the selective inputting means.

The parallel processing paths can further comprise means, coupled between the adder output and the selective inputting means, for truncating the updated coefficients. Means can also be provided between the adder output and the selective inputting means, for adjusting the gain of the updated coefficients. The sets of updated coefficients can be multiplexed to provide a clocked stream of coefficient sets for input to the equalizer filter stage.

In an integrated circuit implementation, the multiplying means can comprise a plurality of multiplying stages corresponding to the plurality of delay stages. The updating means can similarly comprise a plurality of updating stages corresponding to the plurality of delay and multiplying stages. In this manner, sets of corresponding delay, multiplying and updating stages form parallel processing paths for the sets of delayed signal data. The parallel paths are then implemented as slices in an integrated circuit.

Further features and advantages of the present invention are disclosed in the drawings and the detailed description of the embodiments of the invention.

Figure 1 is a block diagram of a typical transmission system illustrating the location of a complex adaptive equalizer;

Figure 2 is a block diagram of an MxN tap complex adaptive equalizer using cascaded components;

Figure 3 is a block diagram of an N-tap complex finite impulse response (FIR) filter that can be used in the equalizer of Figure 2;

Figure 4 is a block diagram illustrating a theoretical FIR filter structure;

Figure 5 is a block diagram illustrating a practical FIR filter structure;

Figure 6 is a block diagram of a coefficient update computation circuit in accordance with the present invention;

Figure 7 is a block diagram of a VLSI implementation of the coefficient update computation circuit of Figure 6;

Figure 8 is a response curve illustrating the convergence time of a prior art complex adaptive equalizer; and

Figure 9 is a response curve illustrating the convergence time of a complex adaptive equalizer in accordance with the present invention.

In the transmission system illustrated in Figure 1, a signal to be transmitted is input to a transmitter 12 via an input terminal 10. The signal contains digital data, modulated on an analog carrier using, for example, well known QAM techniques. The QAM modulated data is a complex signal that includes real components I and im-

aginary components Q. Transmitter 12 is a conventional device, such as a well known VHF or UHF transmitter.

The transmitted signal is communicated via a channel 14, such as a terrestrial VHF or UHF communications channel, to a receiver that contains a quadrature demodulator 16 for the QAM data. Quadrature demodulator 16 is a conventional component that extracts the I and Q components of the received data for input to a complex adaptive equalizer 18. Complex adaptive equalizers, per se, are well known in the art. The present invention provides an improved equalizer with a reduced convergence time using the LMS algorithm. As illustrated in Figure 1, the received channel data input to complex adaptive equalizer 18 is unequalized, and suffers from the intersymbol interference caused by the amplitude and/or delay distortion introduced by communication channel 14. Complex adaptive equalizer 18 compensates for this distortion, and outputs equalized channel data I_{equ} and Q_{equ}. The equalized channel data is input to a conventional decoder 20 to retrieve the transmitted information data, which can comprise, for example, HDTV video information.

Figure 2 illustrates an embodiment of complex adaptive equalizer 18 in greater detail. Unequalized channel data from the quadrature demodulator is input at terminals 30, 32 respectively. Terminal 30 receives the real (I) demodulated channel data and terminal 32 receives the imaginary (Q) demodulated channel data. Each of the demodulated I and Q signals comprise m-bit bytes that are input both to a first stage 34 of N-tap finite impulse response (FIR) filters and a q-bit quantizer 38. Quantizer 38 quantizes each m-bit byte into a smaller byte for input to an N-coefficients update computation circuit 36.

As shown in Figure 2, equalizer 18 comprises M sets or stages, each containing an N-tap FIR filter circuit and an N-coefficients update computation circuit. After the last (Mth) stage, the outputs from the last N-tap FIR filter circuit are combined in adders 40, 42 to provide the real equalized channel data I and the imaginary equalized channel data Q. The equalized I and Q data is also input to an error signal generator 44, which outputs an error signal that is fed back to each of the update computation circuits 36 to 36_M. In a preferred embodiment, error signal generator 44 comprises a programmable read only memory (PROM) that outputs a precalculated stored error value in response to the Q and I data that is used to address the PROM. The stored error values have been previously computed using the well known LMS algorithm.

The last stage N-tap FIR filter circuit 34_M is illustrated in greater detail in Figure 3. As shown, four FIR filter sets 58, 60, 62, and 64 are provided for receiving the real and imaginary channel data from the previous stage. Real data, in the form of m-bit bytes, is received at terminal 50 and input to each of N-tap FIR filters 58, 60. Imaginary data in the form of m-bit bytes is received at terminal 54, for input to N-tap FIR filters 62, 64.

Coefficients generated by the update computation circuits 36 to 36_M (Figure 2) are input to terminals 52 and 56 of the N-tap FIR filter circuit. In particular, terminal 52 receives the real coefficients for input to filters 58 and 64, and terminal 56 receives the imaginary coefficients for input to filters 60 and 62. The outputs of filters 58, 62 are subtracted in an adder 66 to provide the real filter data. The outputs of filters 60, 64 are added in an adder 68 to provide the imaginary filtered data. The operation of such an N-tap FIR filter circuit is described in greater detail in the article to S. U. H. Qureshi referred to above, e.g., at pp. 1355-1356 thereof.

Figure 4 illustrates a theoretical structure of an FIR filter, and is often used to describe such filters. However, the structure of Figure 4 is seldom used in practice, because of the complexities involved in making an N input adder, such as adder 78, and the necessity of providing N delay element outputs, which would require N output pins on an integrated circuit implementation. In the theoretical structure illustrated, data (whether real or imaginary) is input at a terminal 70 to a plurality of successive delay elements 74a, 74b, ... 74n. Coefficient data is input to each of a plurality of terminals 72a, 72b, 72c, ... 72n+1 for application to an associated multiplier 76a, 76b, 76c, ... 76n+1. The multipliers obtain the product of the coefficients with the input data, as successively delayed by delay stages 74a to 74n. The products are summed together in an adder 78 for output to an appropriate adder 66 or 68, illustrated in Figure 3. Thus, the outputs of the N delay elements 74a to 74n, which form a vector of past data, are used in accordance with the LMS algorithm to update the FIR coefficients.

In practice, an FIR filter structure as illustrated in Figure 5 is actually used. Data (real or imaginary) is input at a terminal 80, for application to each of a plurality of multipliers 84a, 84b, 84c, ... 84n. Coefficients are input to each of the multipliers at respective terminals 82a, 82b, 82c,...82n. The products of the input data and the coefficients are input to a respective delay circuit 86a, 86b,... 86n via adders 88a, 88b .... 88n-1, as appropriate. The output of delay circuit 86n comprises the filtered data for input to adder 66 or adder 68 of Figure 3. The operation of the FIR filter is well known in the art.

Generally, only one coeffienct of an FIR filter can be changed for each filter clock cycle. Thus, it takes N filter clock cycles to make one complete adjustment of an N-tap filter. When M, N-tap filters and coefficients update computation circuits are cascaded as illustrated in Figure 2, it still takes only N filter clock cycles to update all MxN taps. In prior art designs, since only one coefficient of the FIR filter is changed each filter clock cycle, all of the other coefficients were maintained at their prior state until the next update cycle for that coefficient arrived. This resulted in a rather long convergence time for an adaptive equalizer utilizing such filters.

The present invention reduces the convergence time of the equalizer by updating all N coefficients each filter clock cycle, even though the FIR filters can accept

only one updated coefficient per filter clock cycle. Since the coefficients are continuously updated, their convergence time is reduced.

The invention implements the LMS algorithm in quantized form to update the coefficients. In unquantized form the algorithm is given by:

$$C_{n+1} = C_n + \Delta E_n X^*_n$$

where C_n is the complex vector of coefficients, X_n is the complex vector of delayed data, * means complex conjugate, E is the complex error signal, and Δ is a scale factor. In quantized form the algorithm is:

$$Q_m[C_{n+1}]=Q_m[C_n]+\delta Q_s[E_n]Q_q[X^*_n]$$

where Q_i is an i-bit quantizer, δ is a scale factor, and the final quantized coefficient is given by $Q_p\{Q_m[C_{n+1}]\}$.

Figure 6 illustrates a 64 tap complex coefficient update computation circuit 36 in accordance with the present invention. Two-bit quantized unequalized complex data (real and imaginary) is input at terminals 90 (real) and 92 (imaginary). Similarly, the two-bit quantized real and imaginary components of a complex error signal are input at terminals 96, 98 respectively. Sixty-four cascaded delay elements 94 receive the real and imaginary data for input, along with the error signals, as addresses to a multiply read-only memory (ROM) that obtains the product of each data component with each error component for input to an accumulator and gain adjust circuit associated with the particular delay element from which the data was output. Circuit 102a is an example of one of the accumulator and gain adjust circuits.

As can be seen in Figure 6, each accumulator and gain adjust circuit 102a to 102n includes a 20-bit accumulator 104 that sums the product from multiply ROM 100 with a delayed product output from delay circuit 106. Delay circuit 106 outputs 20-bit delayed coefficients. The 20-bit accumulator is used to update the coefficients. The LMS scale factor, A , is inherent in the width of the accumulator. After accumulation, the coefficients are truncated and gain adjusted in a conventional truncation and gain adjust circuit 108. The gain adjustment adjusts the magnitude of the coefficients. A multiplexer 110 receives all of the coefficients from the accumulator and gain adjust circuits 102a to 102n, multiplexes them together, and selects one complex coefficient for output to the FIR filter each filter clock cycle. A clock input 112 is provided to input the clock signal to multiplexer 110.

The gain adjustment performed on the truncated coefficients provides a means for improving performance in noise. The values of the less significant coefficients can be limited to minimize random fluctuations about their optimum values.
This minimizes their contribution to the excess error variance, which is an inherent problem with the LMS algorithm.

Figure 7 illustrates an arrangement of the coefficient update computation circuit of Figure 6 that lends itself to a VLSI implementation. As shown in Figure 7, the multiplying means can comprise a plurality of programmable logic array (PLA) multiplying stages 122 corresponding to the plurality of delay elements provided in delay section 94. Each delay elementand PLA multiplication stage corresponds to one of the accumulator and gain adjust stages 102a to 102n, to provide a parallel processing path 120. Each parallel processing path 120 can provide a separate VLSI slice for fabrication in an integrated circuit.

Since the coefficients update computation circuitry of the present invention updates all of the N coefficients in parallel every filter clock cycle, instead of just one coefficient per cycle, the convergence time of the equalizer is not significantly degraded by the practical implementation of the LMS algorithm. Indeed, the convergence time of the invention is on the order of 1/N times the convergence time of prior art schemes that only adjust one coefficient every cycle.

Figures 8 and 9 illustrate the results of two simulations, comparing the convergence times of two equalizers. The prior art equalizer performance illustrated by Figure 8 employs a coefficient update scheme that adjusts only one coefficient every filter clock cycle. Figure 9 illustrates the performance of an equalizer in accordance with the present invention, wherein all N coefficients are updated in parallel every filter clock cycle. The simulations used the quantized version of the LMS algorithm, and a 256 complex taps, fractional spaced equalizer. Both simulations used four, 64 coefficients update computation blocks as illustrated in Figure 6, but the coefficient adjustment for the equalizer pertaining to Figure 8 was limited to one coefficient per filter clock cycle instead of processing all coefficients in parallel. The transmission system was 16-QAM at a symbol rate of 5 MHz, with additive white Gaussian noise (AWGN) and multipath distortion. The carrier-to-noise ratio (C/N) was 30 dB, and the multipath had a reflected ray delayed by 5 microseconds, which was down -10 dB from the direct ray.

The comparison criterion illustrated is the error variance (EV) versus convergence time in symbol periods, where the error is the difference between the received signal point and the nearest 16-QAM constellation point. As can be seen by comparing the response 130 of Figure 8 with the response 140 of Figure 9, a factor of 64 decrease in convergence time (31,250/2,000,000 symbol periods) is obtained by adjusting all the coefficients every filter clock cycle, when compared to adjusting one coefficient every cycle. Thus, the parallel processing of the present invention provides a substantial improvement in performance over the prior art.

It will now be appreciated that the present invention provides an improved equalizer, and in particular a com-

plex adaptive equalizer, wherein convergence time is substantially reduced by updating all of the coefficients in parallel during each filter cycle.

Claims

1. A method for updating coefficients for input to a filter stage (34) of an adaptive equalizer (18), said filter stage (34) receiving one of said updated coefficients during each one of successive filter clock cycles, said coefficients being updated in response to error signals derived from equalized data output from said adaptive equalizer (18), characterized in that:

    a plurality of said coefficients are updated concurrently during each filter clock cycle by passing unequalized data through N successive delay elements (94) to provide a delayed sample of the unequalized data from each of the delay elements;
    the product of each delayed sample output from the delay elements (94) and an error signal derived from equalized data output from said adaptive equalizer (18) is obtained;
    the product corresponding to each delay element is combined with previous product data corresponding to that delay element to produce N updated coefficients during each of said filter clock cycles; and
    during each successive filter clock cycle, one of the N coefficients updated during that cycle is input to said filter stage (34).

2. A method in accordance with claim 1 wherein said equalizer (18) is a complex adaptive equalizer and said signal data, error signal and coefficients include real and imaginary complex components.

3. A method in accordance with claim 1 or 2 comprising the further step of: truncating the coefficients of each updated set.

4. A method in accordance with claim 3 comprising the further step of: adjusting the gain of the truncated coefficients.

5. A method in accordance with claim 4 comprising the further step of: multiplexing the sets of adjusted and/or truncated coefficients to provide a clocked stream of coefficient sets for input to said equalizer filters.

6. A method in accordance with one of the preceding claims comprising the further step of: multiplexing said sets of updated coefficients to provide a clocked stream of coefficients sets for input to said equalizer filters.

7. Adaptive equalizer apparatus comprising a filter stage (34), said filter stage (34) receiving one of updated coefficients during each one of successive filter clock cycles,
updating means (36) for updating said coefficients in response to error signals derived from equalizer data output from said adaptive equalizer (18),
characterized in that

    said updating means (36) comprise a plurality of successive delay elements (94) coupled together to provide a plurality of delayed samples of unequalized signal data which are output for use in updating said coefficients;
    means (100) are provided for multiplying the delayed samples output from said delay elements by an error signal derived from equalized data output from said adaptive equalizer (18), said multiplying means (100) providing a product corresponding to each delay element;
    means (102) are provided for combining the product corresponding to each delay element with previous product data corresponding to that delay element to concurrently produce an updated coefficient corresponding to each delay element during each of said filter clock cycles; and
    means (110) are provided for inputting to said filter stage (34) during each successive filter clock cycle, the updated coefficient corresponding to one of said delay elements.

8. Apparatus in accordance with claim 7 wherein said updating means (36) comprise a plurality of parallel processing paths (102), each path (102) coupled between said multiplying means (100) and said inputting means (110) for updating one of said products.

9. Apparatus in accordance with claim 8 wherein each of said paths (102) comprises:

    an adder (104) having a first input for receiving a product from said multiplying means (100), a second input, and an output;
    a delay circuit (106) coupled to receive product data from said output and to couple delayed product data to said second input; and
    means for coupling said- output to said selective inputting means (110).

10. Apparatus in accordance with claim 9 wherein said paths (102) further comprise:

means (108), coupled between said adder (104) output and said selective inputting means (110) for truncating said updated coefficients.

11. Apparatus in accordance with claim 9 or 10 wherein said paths (102) further comprise:
means (108), coupled between said adder (104) output and said selective inputting means (110), for adjusting the gain of said updated coefficients.

12. Apparatus in accordance with one of claims 7 to 9 further comprising:
means (108) for truncating said updated coefficients.

13. Apparatus in accordance with one of claims 7 to 9 or 12 further comprising:
means (108) for adjusting the gain of said updated coefficients.

14. Apparatus in accordance with one of claims 7 to 13 wherein said inputting means (110) comprise:
means for multiplexing the sets of updated coefficients to provide a clocked stream of coefficients sets for input to said equalizer filter stage (34).

15. Apparatus in accordance with claim 7 wherein:

said multiplying means (100) comprise a plurality of multiplying stages (122) corresponding to said plurality of delay stages;
said updating means (36) comprise a plurality of updating stages corresponding to said plurality of delay and multiplying stages; and
wherein sets of corresponding delay, multiplying and updating stages form parallel processing paths for the sets of delayed signal data.

16. Apparatus in accordance with claim 15 wherein
said parallel paths are implemented as slices in an integrated circuit.

17. Apparatus in accordance with one of claims 7 to 16 wherein
said adaptive equalizer (18) is a complex adaptive equalizer and said signal data, error signal and coefficients include real (I) and imaginary (Q) complex components.

Patentansprüche

1. Verfahren zum Aktualisieren von Koeffizienten zur Eingabe an eine Filterstufe (34) eines adaptiven Entzerrers (18), wobei die Filterstufe (34) einen der aktualisierten Koeffizienten während einem jeden von aufeinanderfolgenden Filtertaktzyklen empfängt, wobei die Koeffizienten als Antwort auf Fehlersignale, welche von einem entzerrten Datenausgangssignal von dem adaptiven Entzerrer (18) abgeleitet werden, aktualisiert werden, dadurch gekennzeichnet, daß eine Mehrzahl der Koeffizienten während jedem Filtertaktzyklus gleichzeitig aktualisiert werden durch Durchlaufen von nicht entzerrten Daten durch N aufeinanderfolgende Verzögerungselemente (94), um eine verzögerte Probe der nicht entzerrten Daten in jedem der Verzögerungselemente bereitzustellen;

das Produkt von jedem verzögerten Probeausgangssignal von den Verzögerungselementen (94) und ein Fehlersignal, welches von dem entzerrten Datenausgangssignal von dem adaptiven Entzerrer (18) abgeleitet wird, erhalten wird;
das Produkt, welches zu jedem der Verzögerungselemente korrespondiert, mit vorhergehenden Produktdaten kombiniert wird, welche mit diesem Verzögerungselement korrespondieren, um N aktualisierte Koeffizienten während jedem der Filtertaktzyklen zu erzeugen;
und während jedem aufeinanderfolgenden Filtertaktzyklus wird einer der N Koeffizienten, welche während dieses Zykluses aktualisiert werden, an die Filterstufe (34) eingegeben.

2. Verfahren nach Anspruch 1, wobei der Entzerrer (18) ein komplexer adaptiver Entzerrer ist, und Signaldaten, Fehlersignal und Koeffizienten komplexe Komponenten mit Real- und Imaginärteil aufweisen.

3. Verfahren nach Anspruch 1 oder 2, welches den weiteren Schritt umfaßt:
Abschneiden der Koeffizienten jedes aktualisierten Satzes.

4. Verfahren nach Anspruch 3, welches den weiteren Schritt umfaßt:
Anpassen der Verstärkung der abgeschnittenen Koeffizienten.

5. Verfahren nach Anspruch 4, welches den weiteren Schritt umfaßt:
Multiplexieren der Sätze von angepaßten und/oder abgeschnittenen Koeffizienten, um einen getakteten Strom von Koeffizientensätzen zur Eingabe an die Entzerrerfilter bereitzustellen.

6. Verfahren nach einem der vorangehenden Ansprüche, welches den weiteren Schritt umfaßt:
Multiplexieren der Sätze von aktualisierten Koeffizienten, um einen getakteten Strom von Koeffizientensätzen zur Eingabe an die Entzerrerfilter bereitzustellen.

7. Adaptiv-Entzerrer-Vorrichtung, welche umfaßt:

eine Filterstufe (34), wobei die Filterstufe (34) einen von aktualisierten Koeffizienten während einem jedem von aufeinanderfolgenden Filtertaktzyklen empfängt,

Aktualisierungsmittel (36) zum Aktualisieren der Koeffizienten als Antwort auf Fehlersignale, welche von einem Entzerrer-Datenausgangssignal von dem adaptiven Entzerrer (18) abgeleitet werden,

dadurch gekennzeichnet, daß die Aktualisierungsmittel (36) eine Mehrzahl von aufeinanderfolgenden Verzögerungselementen (94) umfassen, welche miteinander gekoppelt sind, um eine Mehrzahl von verzögerten Proben von nicht entzerrten Signaldaten bereitzustellen, die zur Verwendung beim Aktualisieren der Koeffizienten ausgegeben werden;

Mittel (100) sind vorgesehen zum Multiplizieren der verzögerten Probeausgangssignale von dem Verzögerungselementen mit einem Fehlersignal, welches vom entzerrten Datenausgangssignal von dem adaptiven Entzerrer (18) abgeleitet ist, wobei die multiplizierenden Mittel (100) ein Produkt bereitstellen, welches zu jedem einzelnen Verzögerungselement korrespondiert.

Mittel (102) sind vorgesehen zum Kombinieren des Produkts, welches zu jedem Verzögerungselement korrespondiert, mit vorhergehenden Produktdaten, die zu diesem Verzögerungselement korrespondieren, um gleichzeitig einen aktualisierten Koeffizienten zu erzeugen, der zu jedem Verzögerungselement während jedem der Filtertaktzyklen korrespondiert;

und Mittel (110) sind vorgesehen zum Eingeben an die Filterstufe (34) während jedem der aufeinanderfolgenden Filtertaktzyklen, wobei der aktualisierte Koeffizient zu einem der Verzögerungselemente korrespondiert.

8. Vorrichtung nach Anspruch 7, wobei die Aktualisierungsmittel (36) eine Mehrzahl von parallelen Verarbeitungspfaden (102) umfassen, wobei jeder Pfad (102) zwischen die multiplizierenden Mittel (100) und den eingebenden Mitteln (110) zum Aktualisieren eines der Produkte gekoppelt ist.

9. Vorrichtung nach Anspruch 8, wobei jeder der Pfade (102) umfaßt:

einen Addierer (104), welcher einen ersten Eingang zum Empfangen eines Produkts von den multiplizierenden Mitteln (100), einen zweiten Eingang und einen Ausgang aufweist;

einen Verzögerungskreis (106), welcher angekoppelt ist, um Produktdaten von dem Ausgang zu empfangen und um die verzögerten Produktdaten an den zweiten Eingang zu koppeln; und

Mittel zum Koppeln des Ausgangs an die auswählenden eingebenden Mittel (110).

10. Vorrichtung nach Anspruch 9, wobei die Pfade (102) weiter umfassen:
Mittel (108), die zwischen den Addierer (104)-Ausgang und die selektiven eingebenden Mitteln (110) gekoppelt sind, um die aktualisierten Koeffizienten abzuschneiden.

11. Vorrichtung nach Anspruch 9 oder 10, wobei die Pfade (102) weiter umfassen:
Mittel (108), welche zwischen den Addierer (104)-Ausgang und die selektiven eingebenden Mittel (110) gekoppelt sind, zum Anpassen der Verstärkung der aktualisierten Koeffizienten.

12. Vorrichtung nach einem der Ansprüche 7 bis 9, welche weiter umfaßt:
Mittel (108) zum Abschneiden der aktualisierten Koeffizienten.

13. Vorrichtung nach einem der Ansprüche 7 bis 9 oder 12, welche weiter umfaßt:
Mittel (108) zum Anpassen der Verstärkung der aktualisierten Koeffizienten.

14. Vorrichtung nach einem der Ansprüche 7 bis 13, wobei die eingebenden Mittel (110) umfassen:
Mittel zum Multiplexieren der Sätze von aktualisierten Koeffizienten, um einen getakteten Strom von Koeffizientensätzen zur Eingabe an die Entzerrer-Filterstufe (34) bereitzustellen.

15. Vorrichtung nach Anspruch 7, wobei die multiplizierenden Mittel (100) eine Mehrzahl von multiplizierenden Stufen (122), welche zu der Mehrzahl von Verzögerungsstufen korrespondieren, umfassen;

die Aktualisierungsmittel (36) umfassen eine Mehrzahl von Aktualisierungsstufen, die zu der Mehrzahl von Verzögerungsstufen und multiplizierenden Stufen korrespondieren; und

wobei Sätze von korrespondierenden Verzögerungs-, multiplizierenden und aktualisierenden Stufen parallele Verarbeitungspfade für die Sätze von verzögerten Signaldaten bilden.

16. Vorrichtung nach Anspruch 15, wobei die parallelen Pfade als Scheiben in einen integrierten Schaltkreis implementiert sind.

17. Vorrichtung nach einem der Ansprüche 7 bis 16, wobei der adaptive Entzerrer (18) ein komplexer adaptiver Entzerrer ist und die Signaldaten, Fehlersignal und Koeffizienten komplexe Koeffizienten mit Realteil (I) und Imaginärteil (Q) umfassen.

Revendications

1. Procédé pour la mise à jour de coefficients à introduire dans un étage de filtre (34) d'un égaliseur adaptatif (18), l'étage de filtre (34) recevant pendant chacun des cycles successifs d'horloge de filtre un des coefficients mis à jour, les coefficients étant mis à jour en réponse à des signaux d'erreur dérivés de données compensées délivrées par l'égaliseur adaptatif (18), caractérisé en ce que :

   une pluralité desdits coefficients sont mis à jour concurremment pendant chaque cycle d'horloge de filtre en faisant passer des données non compensées à travers N éléments de retard (94) successifs afin de fournir un échantillon retardé des données non compensées en provenance de chacun des éléments de retard,
   le produit de chaque échantillon retardé délivré par les éléments de retard (94) et d'un signal d'erreur dérivé de données compensées émises par l'égaliseur adaptatif (18) est obtenu,
   le produit correspondant à chaque élément de retard est combiné à des données de produits précédents correspondant à cet élément de retard, afin de produire, pendant chacun des cycles d'horloge de filtre, N coefficients mis à jour, et
   pendant chaque cycle successif d'horloge de filtre, un des N coefficients mis à jour pendant ce cycle est introduit dans l'étage de filtre (34).

2. Procédé suivant la revendication 1, caractérisé en ce que l'égaliseur (18) est un égaliseur adaptatif complexe et en ce que les données de signal, le signal d'erreur et les coefficients comprennent des composantes complexes réelles et imaginaires.

3. Procédé suivant la revendication 1 ou 2, caractérisé en ce qu'il comprend l'étape supplémentaire de tronquer les coefficients de chaque ensemble mis à jour.

4. Procédé suivant la revendication 3, caractérisé en ce qu'il comprend l'étape supplémentaire de régler le gain des coefficients tronqués.

5. Procédé suivant la revendication 4, caractérisé en ce qu'il comprend l'étape supplémentaire de multiplexer les ensembles de coefficients réglés et/ou tronqués, afin de fournir un train rythmé d'ensembles de coefficients à introduire dans lesdits filtres d'égaliseur.

6. Procédé suivant l'une des revendications précédentes, caractérisé en ce qu'il comprend l'étape supplémentaire de multiplexer les ensembles de coefficients mis à jour afin de fournir un train rythmé d'ensembles de coefficients à introduire dans les filtres d'égaliseur.

7. Dispositif d'égaliseur adaptatif comprenant

   un étage de filtre (34), l'étage de filtre (34) recevant un des coefficient mis à jour pendant chacun des cycles successifs d'horloge du filtre,
   des moyens de mise à jour (36) pour mettre à jour lesdits coefficients en réponse à des signaux d'erreur dérivés de données d'égaliseur délivrées par l'égaliseur adaptatif (18),

   caractérisé en ce que :

   les moyens de mise à jour (36) comprennent une pluralité d'éléments de retard successifs (94) raccordés ensemble pour fournir une pluralité d'échantillons retardés de données de signal non compensé qui sont délivrées pour être utilisées pour la mise à jour desdits coefficients,
   des moyens (100) sont prévus pour multiplier les échantillons retardés, délivrés par les éléments de retard précités, par un signal d'erreur dérivé de données compensées délivrées par l'égaliseur adaptatif (18), les moyens de multiplication (100) fournissant un produit correspondant à chaque élément de retard,
   des moyens (102) sont prévus pour combiner le produit correspondant à chaque élément de retard à des données de produits précédents correspondant à cet élément de retard, afin de produire concurremment pendant chacun des cycles d'horloge de filtre un coefficient mis à jour qui correspond à chaque élément de retard, et
   des moyens (110) sont prévus pour introduire dans l'étage de filtre (34), pendant chaque cycle successif d'horloge du filtre, le coefficient mis à jour correspondant à un desdits éléments de retard.

8. Dispositif suivant la revendication 7, caractérisé en ce que les moyens de mise à jour (36) comprennent une pluralité de trajets de traitement parallèles (102), chaque trajet (102) étant raccordés entre les

moyens de multiplication (100) et les moyens d'introduction (110) afin de mettre à jour un des produits susdits.

9. Dispositif suivant la revendication 8, caractérisé en ce que chacun des trajets (102) comprend :

un additionneur (104) présentant une première entrée pour recevoir un produit en provenance des moyens de multiplication (100), une seconde entrée et une sortie,
un circuit de retard (106) raccordé pour recevoir des données de produit en provenance de ladite sortie et pour coupler à la seconde entrée précitée les données de produit retardées, et
des moyens pour raccorder ladite sortie aux moyens d'introduction sélective (110).

10. Dispositif suivant la revendication 9, caractérisé en ce que les trajets (102) comprennent en outre des moyens (108) raccordés entre la sortie de l'additionneur (104) et les moyens d'introduction sélective (110) en vue de tronquer les coefficients mis à jour.

11. Dispositif suivant la revendication 9 ou 10, caractérisé en ce que les trajets (102) comprennent en outre des moyens (108) raccordés entre la sortie de l'additionneur (104) et les moyens d'introduction sélective (110), afin de régler le gain des coefficients mis à jour précités.

12. Dispositif suivant l'une des revendications 7 à 9, caractérisé en ce qu'il comprend en outre des moyens (108) pour tronquer les coefficients mis à jour.

13. Dispositif suivant l'une des revendications 7, 8, 9, 12, caractérisé en ce qu'il comprend en outre des moyens (108) pour régler le gain des coefficients mis à jour.

14. Dispositif suivant l'une des revendications 7 à 13, caractérisé en ce que les moyens d'introduction (110) comprennent des moyens pour multiplexer les ensembles de coefficients mis à jour, afin de fournir un train rythmé d'ensembles de coefficients à introduire dans l'étage de filtre de l'égaliseur (34).

15. Dispositif suivant la revendication 7, caractérisé en ce que:

les moyens de multiplication (100) comprennent une pluralité d'étage de multiplication (122) correspondant à la pluralité d'étages de retard,
les moyens de mise à jour (36) comprennent une pluralité d'étages de mise à jour correspondant à la pluralité d'étages de retard et de multiplication, et
des ensembles d'étages correspondants de retard, de multiplication et de mise à jour forment des trajets de traitement parallèles pour les ensembles de données de signal retardé.

16. Dispositif suivant la revendication 15, caractérisé en ce que les trajets parallèles susdits sont réalisés sous forme de tranches dans un circuit intégré.

17. Dispositif suivant l'une des revendications 7 à 16, caractérisé en ce que l'égaliseur adaptatif (18) est un égaliseur adaptatif complexe et en ce que les données de signal, le signal d'erreur et les coefficients comprennent des composantes complexes réelles (I) et imaginaires (Q).

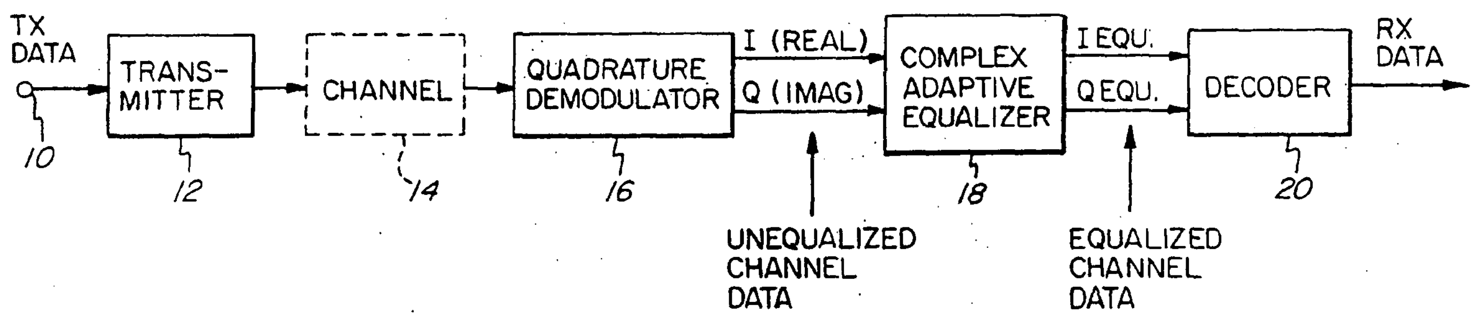
TX DATA
10
TRANS-MITTER
12
CHANNEL
14
QUADRATURE DEMODULATOR
16
I (REAL)
Q (IMAG)
UNEQUALIZED CHANNEL DATA
COMPLEX ADAPTIVE EQUALIZER
18
I EQU.
Q EQU.
EQUALIZED CHANNEL DATA
DECODER
20
RX DATA

FIG. 1

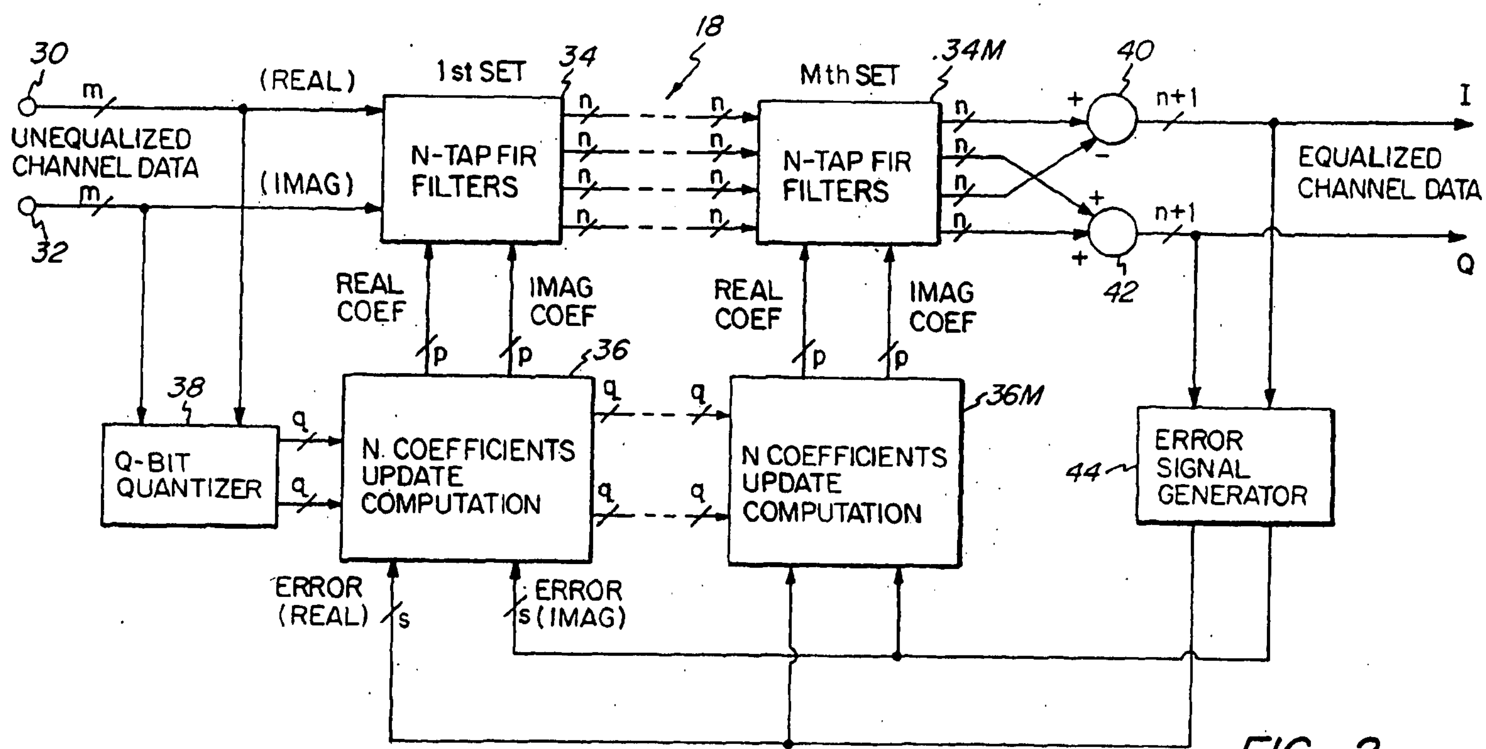
30
m
(REAL)
UNEQUALIZED
CHANNEL DATA
m
(IMAG)
32
1st SET
34
N-TAP FIR
FILTERS
18
Mth SET
.34M
N-TAP FIR
FILTERS
n
n
n
n
40
42
n+1
n+1
I
Q
EQUALIZED
CHANNEL DATA
REAL
COEF
IMAG
COEF
p
p
36
36M
38
Q-BIT
QUANTIZER
q
q
N. COEFFICIENTS
UPDATE
COMPUTATION
N COEFFICIENTS
UPDATE
COMPUTATION
44
ERROR
SIGNAL
GENERATOR
ERROR
(REAL)
s
ERROR
s (IMAG)
+
-
+
+

FIG. 2

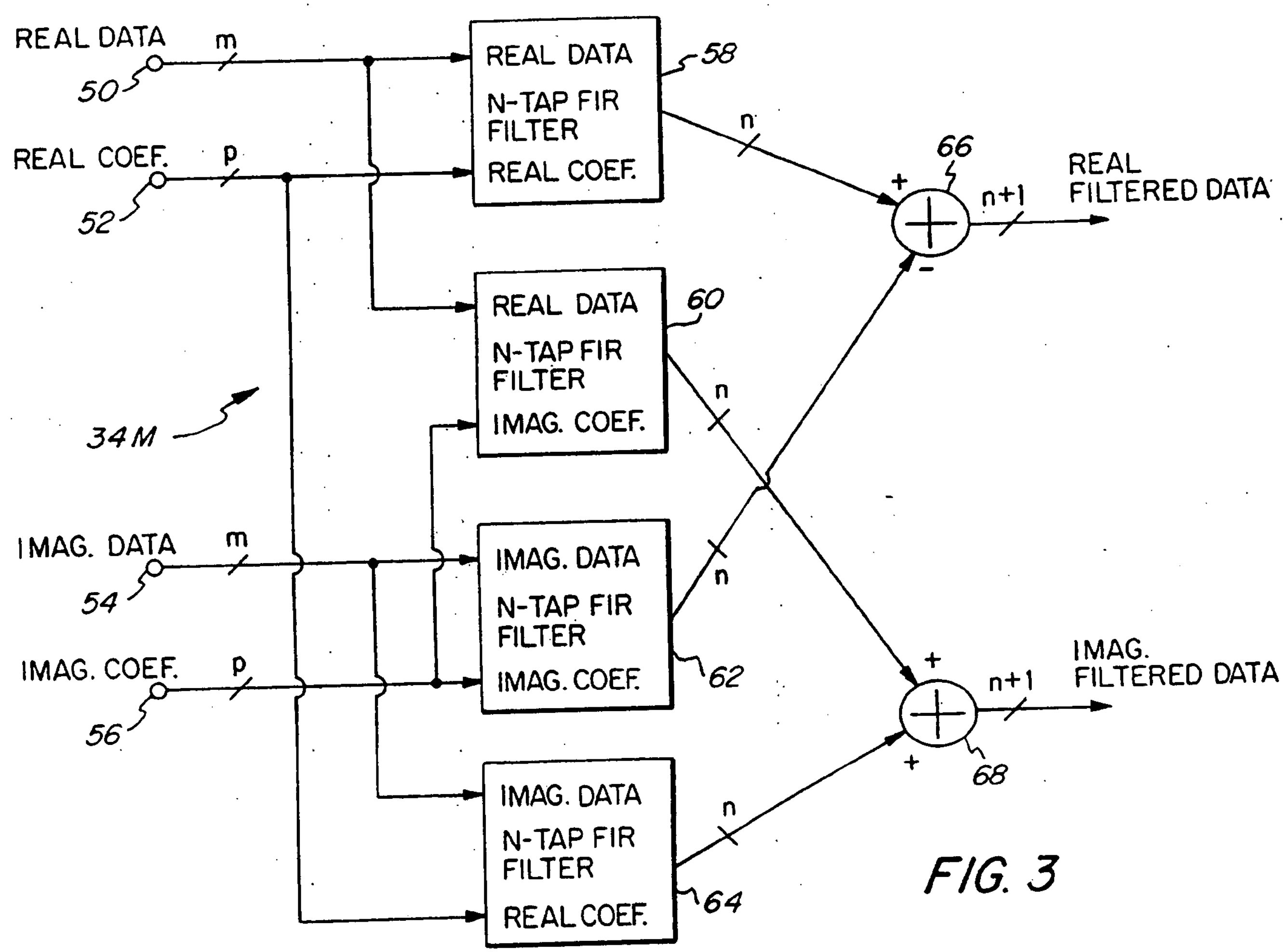
REAL DATA
50
m
REAL COEF.
52
p
REAL DATA
N-TAP FIR
FILTER
REAL COEF.
58
REAL DATA
N-TAP FIR
FILTER
IMAG. COEF.
60
34M
IMAG. DATA
54
m
IMAG. COEF.
56
p
IMAG. DATA
N-TAP FIR
FILTER
IMAG. COEF.
62
IMAG. DATA
N-TAP FIR
FILTER
REAL COEF.
64
n
n
n
n
+
-
66
n+1
REAL
FILTERED DATA
+
+
68
n+1
IMAG.
FILTERED DATA

FIG. 3

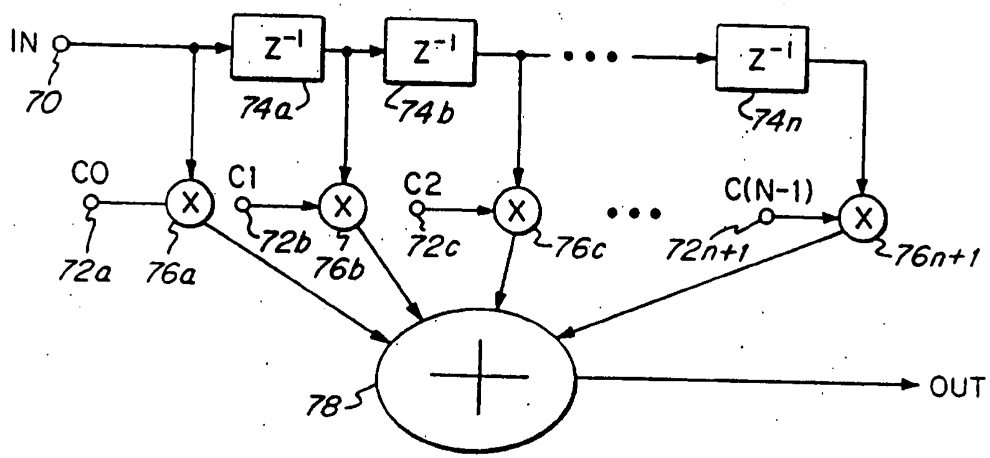
IN
70
74a
74b
74n
CO
C1
C2
C(N-1)
72a
76a
72b
76b
72c
76c
72n+1
76n+1
78
OUT

FIG. 4

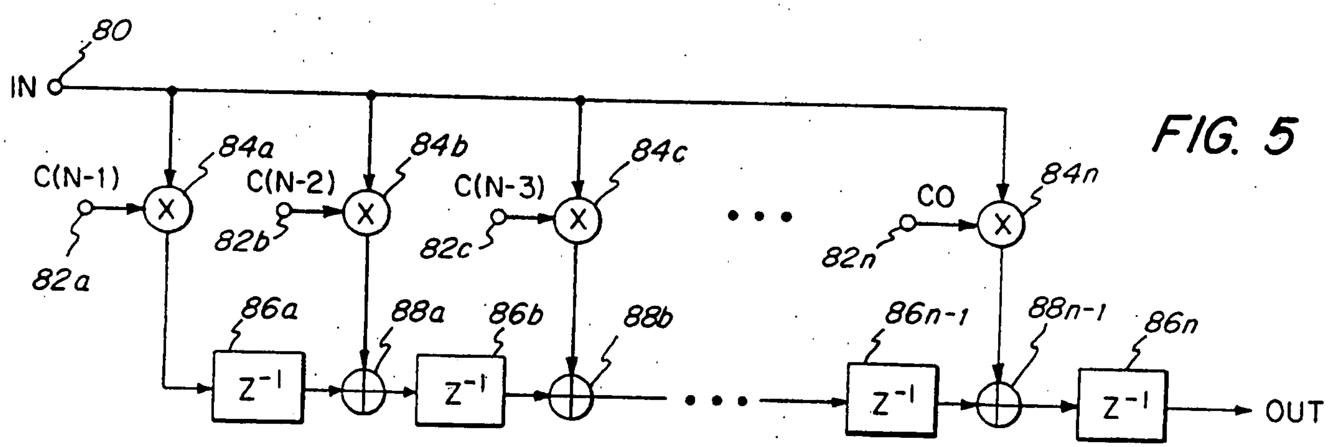
IN
80
C(N-1)
C(N-2)
C(N-3)
CO
82a
82b
82c
82n
84a
84b
84c
84n
86a
88a
86b
88b
86n-1
88n-1
86n
OUT

FIG. 5

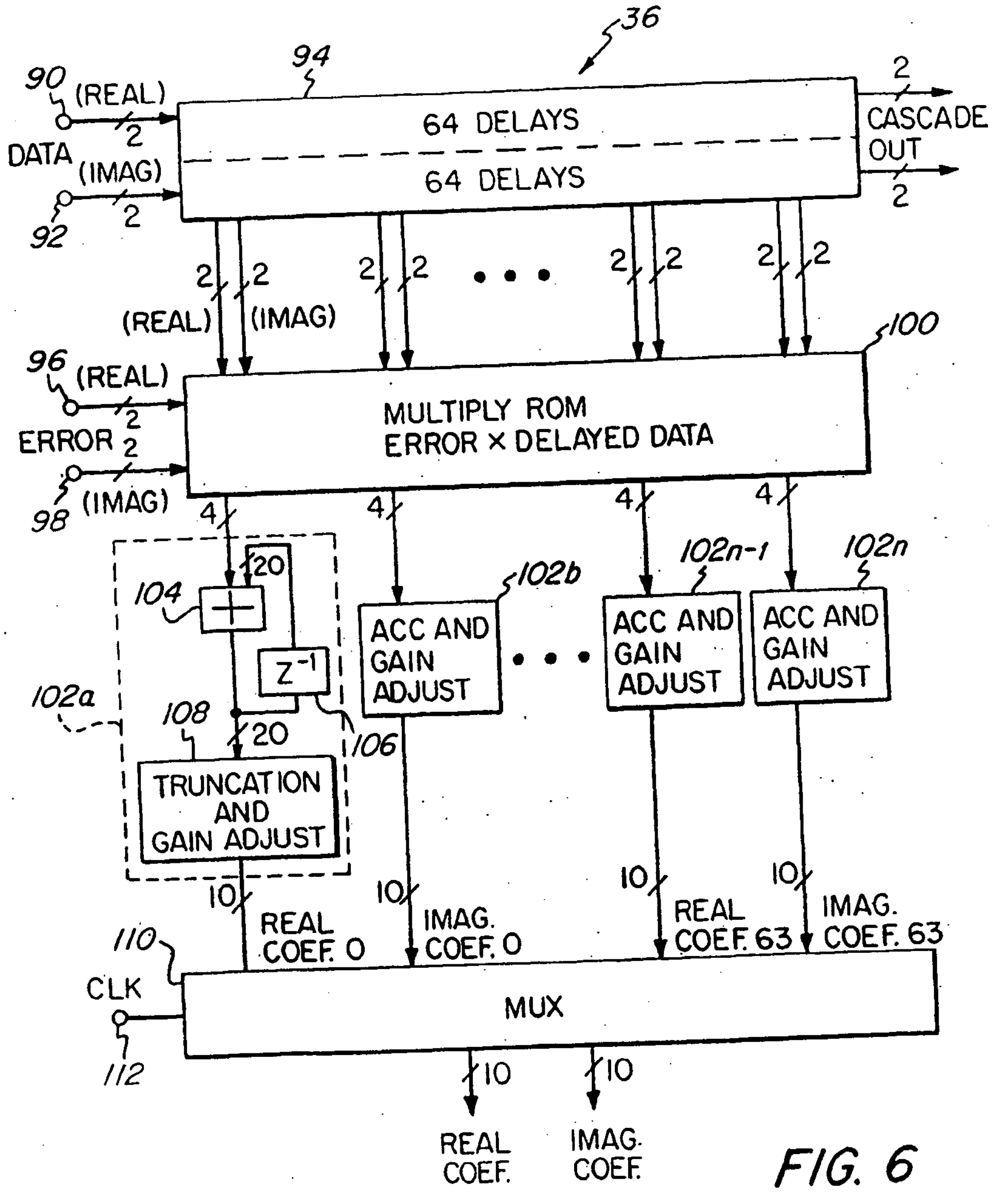
36
94
90
(REAL)
2
DATA
(IMAG)
2
92
64 DELAYS
64 DELAYS
2
CASCADE
OUT
2
(REAL)
(IMAG)
100
96
(REAL)
ERROR
98
(IMAG)
MULTIPLY ROM
ERROR × DELAYED DATA
4
20
104
102a
108
20
106
TRUNCATION
AND
GAIN ADJUST
102b
ACC AND
GAIN
ADJUST
102n-1
ACC AND
GAIN
ADJUST
102n
ACC AND
GAIN
ADJUST
10
REAL
COEF. 0
IMAG.
COEF. 0
REAL
COEF. 63
IMAG.
COEF. 63
110
CLK
112
MUX
10
REAL
COEF.
IMAG.
COEF.

FIG. 6

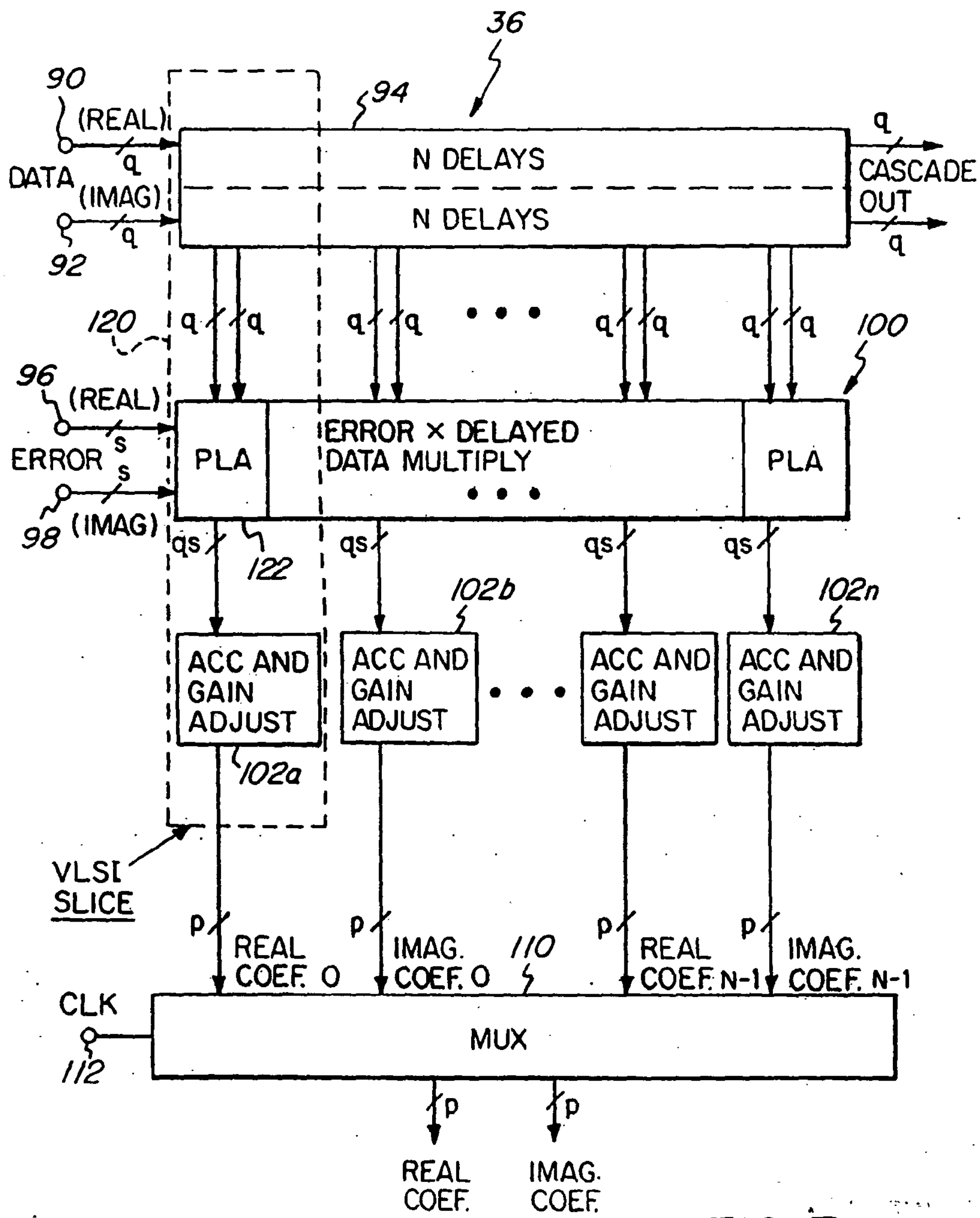
36
94
90
(REAL)
q
DATA
(IMAG)
q
92
N DELAYS
N DELAYS
q
CASCADE
OUT
q
120
q q q q q q q q
100
96
(REAL)
s
ERROR
s
98
(IMAG)
PLA
ERROR × DELAYED
DATA MULTIPLY
PLA
qs
122
qs
qs
qs
102b
102n
ACC AND
GAIN
ADJUST
ACC AND
GAIN
ADJUST
ACC AND
GAIN
ADJUST
ACC AND
GAIN
ADJUST
102a
VLSI
SLICE
p
REAL
COEF. O
p
IMAG.
COEF. O
110
p
REAL
COEF. N-1
p
IMAG.
COEF. N-1
CLK
112
MUX
p
p
REAL
COEF.
IMAG.
COEF.

FIG. 7

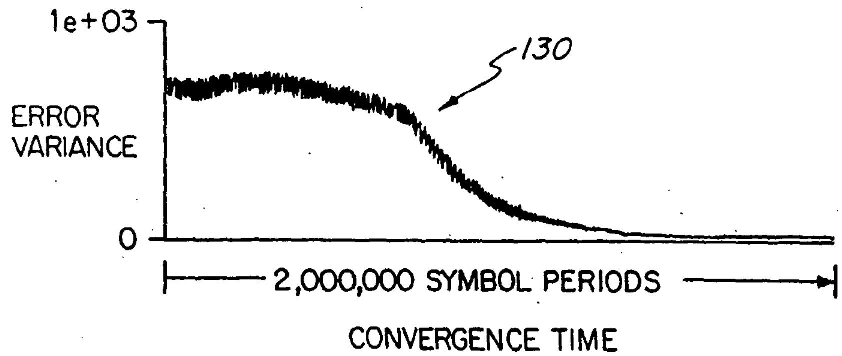

FIG. 8
(PRIOR ART)

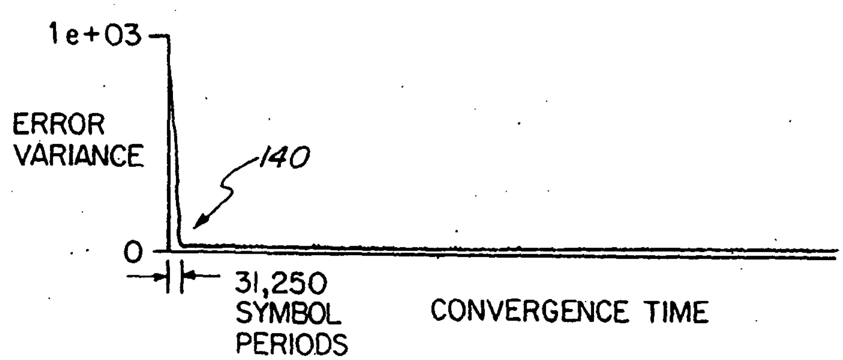

FIG. 9

DOCKET NO: L&L-I0350
SERIAL NO: ____
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